1. How many total digital input/output pins does the XEM 7310-A75 board have?
   1. 126 user pins - 2 sets of 80 connectors
2. What is the maximum clocking speed of the XEM 7310-A75 board?
   1. 200 Mhz
3. How does the XEM 6002 board compare to XEM 7310-A75 in terms of logic gate count, transfer speeds between the board and PC, external memory, and clocking speed of digital logic?

|  | XEM 6002 | XEM 7310-A75 |
| --- | --- | --- |
| Logic Gate Count | Medium Gate count |  |
| Transfer Speed | 36 MBytes/Second | 340 MiBytes/Second |
| External Memory | 32 Mb SPI | 1 GiByte DDR3 |
| Clocking Speed | 1 MHz - 150 MHz | 200Mhz |

1. Why is the *clkdiv* register 24-bit long?
   1. The reason for the clkdiv being 24 bits is because it is being divided by 10,000,000 so that the 20MHz clock will run at 2 Hz
2. If *clkdiv* is declared as an 8-bit register, what is the minimum frequency you can achieve for the *slow\_clk* signal using these FSMs?
   1. 78
3. Look at the Project Summary window. In the Utilization section, you will find out the number of look up tables (LUT), flip flops (FF), input/output pins (IO) and buffers (BUFG) are used for your design. How many resources on the FPGA are used to implement your code?
   1. 34 LUT, 40 FF, 10 IO, BUFG 1
4. Include a printout of your Verilog code with your report.
   1. 